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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/646,076

08/22/2003

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NVID-P000705

9603

45594

7590

06/04/2008

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EXAMINER

HSU, JONI

ART UNIT

PAPER NUMBER

2628

MAIL DATE

DELIVERY MODE

06/04/2008

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/646,076	<b>Applicant(s)</b> MONTRYM ET AL.	
	<b>Examiner</b> JONI HSU	<b>Art Unit</b> 2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 19 February 2008.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-25 and 27-44 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-23, 25, 27-35 and 38-42 is/are rejected.
- 7) ☒ Claim(s) 24, 36, 37, 43 and 44 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

**DETAILED ACTION*****Response to Arguments***

1. Applicant's arguments filed February 19, 2008 are considered but not persuasive.
2. As per Claim 28, Applicant argues Johns (US006366289B1) teaches away from claims by teaching virtual frame buffer which performs pixel-to-pixel mapping instead of pixel-to-multiple subpixel mapping as claimed (p. 14-15).

In reply, Fuchs is used to teach pixel-to-multiple subpixel mapping (p. 119, 2<sup>nd</sup> col., 4<sup>th</sup> para.). Fuchs does not teach virtual frame buffer. But, Johns is used to teach virtual frame buffer (c. 16, ll. 15-23, 55-67). Johns teaches this is advantageous because display image being managed as virtual frame buffer appears as if it resides in frame buffer address space, but in actuality, display image is sub-divided into chunks distributed randomly in memory (c. 6, ll. 58-61), which requires less memory than conventional frame buffer (c. 2, ll. 11-14, 53-66). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Fuchs so it uses virtual frame buffer to perform the pixel-to-multiple subpixel mapping as suggested by Johns so display image appears as if it resides in frame buffer address space, but in actuality, display image is sub-divided into chunks distributed randomly in memory, which requires less memory than conventional frame buffer. So, combination of Fuchs and Johns teaches virtual frame buffer which performs pixel-to-multiple subpixel mapping.

3. Applicant argues Morein (US006188394B1), Fuchs, and Johns do not teach wherein each of multiple subpixel addresses comprise mapped subpixel addresses and mapped subpixel addresses which were transformed from pixel address (p. 15).

In reply, Examiner points out Fuchs teaches pixel address (x, y) is subdivided into grid of subpixels so each subpixel has address of form (x+xoffset, y+yoffset) (p. 119, 2<sup>nd</sup> col., 4<sup>th</sup> para). So, each subpixel in grid of multiple subpixels has different xoffset and different yoffset, so each subpixel has different address. So, received address (x, y) is transformed into multiple subpixel addresses since each of multiple subpixels has different address in form (x+xoffset, y+yoffset) since each of multiple subpixels has different xoffset and different yoffset. Fuchs teaches using 2 subpixel addresses to read 2 subpixels (p. 119, 2<sup>nd</sup> col., 4<sup>th</sup> para). So, Fuchs does teach wherein each of multiple subpixel addresses comprise mapped subpixel addresses and mapped subpixel addresses which were transformed from pixel address.

4. As per Claim 1, Applicant argues Morein teaches away from claims by teaching subpixel-to-subpixel address transformation instead of pixel-to-subpixel address transformation as claimed (p. 18).

In reply, Examiner points out Claim 1 recites "...transforming the memory address into at least one physical address within a frame buffer utilized for antialiasing, wherein memory address is associated with a pixel, wherein said at least one physical address is associated with a plurality of subpixels..." Morein teaches pointer that is stored in **buffer location** (memory address) corresponding to particular pixel points to selected address (physical address) in sample memory (frame buffer) utilized for antialiasing (c. 2, ll. 10-11, 18-22). So, pointer translates or transforms buffer location (memory address) that it is stored in into selected address (physical address) in sample memory (frame buffer) utilized for antialiasing (c. 2, ll. 10-11, 18-22), wherein memory

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address is associated with a pixel (c. 2, ll. 19-20), wherein at least 1 physical address is associated with plurality of subpixels (c. 2, ll. 10-11, 18-22), as recited in Claim 1.

5. As per Claim 5, Applicant argues Liang (US 20020140655A1) teaches away from claims by teaching pitch value in units of physical distance instead of pitch value in address units as claimed (p. 20).

In reply, Examiner points out Dye (US005664162A) is used to teach pitch value of frame buffer (110, Fig. 1) (c. 7, ll. 59-66; c. 9, ll. 59-64; c. 12, ll. 10-17). But, Dye does not teach pitch value comprises distance between two of plurality of subpixels. But, Liang teaches pitch value comprises distance between two of plurality of subpixels [0002]. But, Liang does not expressly teach frame buffer. Since Dye expressly teaches frame buffer that stores image to be displayed within its address space (c. 1, ll. 40-41; c. 11, ll. 31-44), teaching from Liang can be incorporated into Dye so that pitch value of frame buffer comprises distance in address units between 2 of plurality of subpixels, wherein image from frame buffer is displayed. So, combination of Dye and Liang teaches pitch value comprises distance in address units between 2 of plurality of subpixels.

### ***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

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1. Determining the scope and contents of the prior art.
  2. Ascertaining the differences between the prior art and the claims at issue.
  3. Resolving the level of ordinary skill in the pertinent art.
  4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
8. Claims 1-4, 9, 10, 13, 15-17, 19, 21-23, and 32-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morein (US006188394B1) and Johns (US006366289B1).
9. As per Claim 1, Morein teaches method for providing antialiased memory access (c. 2, ll. 46-47; c. 4, ll. 9-13), method comprising receiving request to access memory address (c. 4, ll. 9-13). Pointer that is stored in **buffer location** (memory address) corresponding to particular pixel points to selected address (physical address) in sample memory (frame buffer) utilized for antialiasing (c. 2, ll. 10-11, 18-22). So, pointer translates or transforms buffer location (memory address) that it is stored in into selected address (physical address) in sample memory (frame buffer) utilized for antialiasing (c. 2, ll. 10-11, 18-22), memory address is associated with pixel (c. 2, ll. 19-20), at least 1 physical address is associated with plurality of subpixels for pixel and generated using frame buffer 36 (c. 2, ll. 19-23), frame buffer (sample memory 38) is single memory having data associated with plurality of subpixels (samples), plurality of subpixels correspond to at least 1 pixel of frame buffer 36 (c. 2, ll. 19-23, 25-31); accessing data associated with subpixel at least 1 physical address within frame buffer (c. 4, ll. 9-13).

But, Morein does not teach frame buffer 36 is virtual frame buffer and determining if memory address is in virtual frame buffer, if so, performing transforming and accessing. But, Johns teaches if memory address is in virtual frame buffer, memory address is transformed and driver manages memory to access data at transformed address

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(c. 16, ll. 15-23, 55-67), if memory address is not in virtual frame buffer, then driver manages memory to access data at memory address (c. 15, ll. 56-62). So, since different operations are performed depending on whether or not memory access is within virtual frame buffer, this means there is determination as to whether memory access is within virtual frame buffer. Johns teaches determining if memory address is within virtual frame buffer and, if so, performing transforming and accessing (c. 16, ll. 15-23, 55-67). One physical address is associated with pixel and generated using virtual frame buffer (c. 16, ll. 15-23, 55-67). This teaching from Johns is incorporated into Morein. So, frame buffer 36 of Morein is modified so it is operated as virtual frame buffer in manner taught by Johns. Since Johns teaches one physical address is associated with pixel and Morein teaches one physical address is associated with plurality of subpixels for pixel, when teaching of virtual frame buffer from Johns is incorporated into Morein, combination teaches that one physical address is associated with plurality of subpixels.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify Morein to include virtual frame buffer because Johns teaches display image being managed as virtual frame buffer appears as if it resides in frame buffer address space, but in actuality, display image is sub-divided into chunks distributed randomly in memory (c. 6, ll. 58-61), which requires less memory than conventional frame buffer (c. 2, ll. 11-14, 53-66).

10. As per Claims 2 and 22, Morein does not teach accessing data at memory address provided the memory address is not within virtual frame buffer. However, Johns teaches if memory address is within virtual frame buffer, memory address is transformed into physical address within frame buffer, and driver manages memory to access data at

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physical address within frame buffer (c. 16, ll. 15-23, 55-67). If memory address is not within virtual frame buffer, then driver manages memory to access data at memory address (c. 15, ll. 56-62).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Morein to include accessing data at memory address provided the memory address is not within virtual frame buffer because Johns suggests advantage of using video memory for frame buffer as well as for other clients such as compositor (c. 7, ll. 36-51; c. 9, ll. 31-33). If video memory is being accessed for frame buffer, then it is advantageous to use virtual frame buffer, as discussed for Claim 1. If video memory is being accessed for other clients such as compositor, then video memory can be directly accessed by compositor (c. 8, ll. 30-33).

11. As per Claims 3, 13, 19, and 23, Morein does not teach virtual frame buffer has predefined memory range of graphics memory. However, Johns teaches virtual frame buffer has predefined memory range of graphics memory (310, Fig. 3) (c. 16, ll. 15-23, 55-67; c. 15, ll. 56-62; c. 7, ll. 48-51). This would be obvious for reasons for Claim 2.

12. As per Claim 4, Morein teaches memory address received from CPU (82; c. 8, ll. 43-45).

13. As per Claim 9, it is similar to Claim 1, except that Claim 9 is for accessing data in order to read data. Morein teaches accessing data in order to read data (c. 4, ll. 9-13).

14. As per Claim 10, Morein teaches providing subpixel value to CPU (82; c. 8, ll. 43-52).

15. As per Claim 15, it is similar in scope to Claim 9, except it is for computer system further having at least one peripheral device coupled to processor coupled to memory,



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reading plurality of subpixel values and combining subpixel values. Morein teaches computer system having processor (82, Fig. 4) coupled to memory (94) (c. 8, ll. 43-45), reading plurality of subpixel (sample) values at plurality of physical addresses within frame buffer (38, Fig. 2; c. 4, ll. 9-13; c. 2, ll. 19-23), combining subpixel values to generate pixel value for specific pixel (c. 2, ll. 25-31).

But, Morein does not teach computer system further has at least one peripheral device coupled to the processor. But, Johns teaches computer system has at least one peripheral device (40, 42, 49, Fig. 1) coupled to processor (20) (c. 4, ll. 67-c. 5, ll. 17).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Morein so computer system further has at least one peripheral device coupled to processor because Johns suggests these peripheral devices are needed in order for user to communicate with processor (c. 4, ll. 67-c. 5, ll. 17).

16. As per Claim 16, Morein teaches providing pixel value to CPU (82; c. 8, ll. 21-25).

17. As per Claim 17, Morein teaches that the combining comprises blending the subpixel values into a single color value (c. 2, ll. 25-31).

18. As per Claim 21, it is similar to Claim 1, except Claim 21 is for accessing data in order to write data. Morein teaches accessing data in order to write data (c. 2, ll. 15-19).

19. As per Claim 32, Morein teaches receiving address in frame buffer 36 from computer program (c. 5, ll. 39-48; c. 9, ll. 64-c. 10, ll. 20); transforming received address into at least one subpixel (sample) address (c. 5, ll. 39-48; c. 5, ll. 59-c. 6, ll. 2), subpixel address being address into frame buffer (sample memory 38) which is single memory storing data of plurality of subpixels corresponding to each pixel of frame buffer 36,

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wherein the subpixel address is generated using frame buffer 36 (c. 2, ll. 19-23, 25-31); reading at least two subpixels from frame buffer (sample memory 38) using subpixel address (c. 4, ll. 9-14); blending at least two subpixels to create pixel value (c. 2, ll. 25-31); supplying created pixel value to computer program as if it were pixel value located at received address in frame buffer 36; computer program does not directly access frame buffer (sample memory 38) (c. 4, ll. 9-14).

However, Morein does not teach frame buffer 36 is virtual frame buffer, and supplying base address and buffer size information corresponding to virtual frame buffer. However, Johns teaches method for supplying virtual frame buffer to computer program, the method comprising supplying base address and buffer size information to computer program, base address and buffer size information corresponding to virtual frame buffer (c. 10, ll. 27-30; c. 16, ll. 34-44); receiving address in virtual frame buffer from computer program (c. 16, ll. 59-64); transforming received address (c. 17, ll. 1-3); reading data using transformed address; supplying data to computer program as if it were pixel value located at received address in virtual frame buffer; and wherein computer program does not directly access frame buffer (c. 6, ll. 52-61).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Morein to include supplying base address and buffer size information corresponding to virtual frame buffer as suggested by Johns. Johns suggests base address is needed in order to know where frame buffer starts, all addresses can be calculated by adding certain offset to base address, which simplifying calculation of which chunk contains requested pixel address. Buffer size is needed in order to

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calculate correct address (c. 16, ll. 34-44). Advantages of using virtual frame buffer were discussed for Claim 1.

20. As per Claim 33, Morein does not teach the computer program is an operating system. But, Johns teaches computer program is operating system (35) (c. 4, ll. 64-67).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Morein so program is operating system because Johns teaches it is well-known in art to use operating system software to perform operations on memory (c. 1, ll. 42-51).

21. As per Claim 34, Morein does not teach that the computer program is a software driver. However, Johns teaches the computer program is software driver (c. 13, ll. 8-20).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Morein to include software driver because Johns teaches using this driver allows host to choose memory managing scheme (c. 13, ll. 8-20), making scheme more flexible.

22. As per Claim 35, Morein teaches program 84 is application program (c. 8, ll. 16-21).

23. Claims 5, 6, 11, 12, 18, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morein (US006188394B1) and Johns (US006366289B1) in view of Dye (US005664162A), further in view of Liang (US 20020140655A1).

24. As per Claims 5 and 11, Morein and Johns are relied on for teachings for Claim 4.

However, Dye describes providing the CPU (128, Fig. 1) with a pitch value of the frame buffer (110) (c. 7, ll. 59-66; c. 9, ll. 59-64; c. 12, ll. 10-17).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify Morein and Johns to include providing CPU with pitch value of frame buffer because Dye teaches CPU needs to know pitch value of frame buffer in order to read data from correct location corresponding with virtual frame buffer (116) (c. 3, ll. 49-51; c. 12, ll. 1-24).

However, Morein, Johns, and Dye do not teach that the pitch value comprises a distance in address units between two of the plurality of subpixels. However, Liang teaches that the pitch value comprises a distance between two of the plurality of subpixels [0002]. However, Liang does not expressly teach frame buffer. Since Dye expressly teaches frame buffer that stores image to be displayed within its address space (c. 1, ll. 40-41; c. 11, ll. 31-44), teaching from Liang can be incorporated into device of Dye so that pitch value of frame buffer comprises distance in address units between two of plurality of subpixels, wherein image from frame buffer is displayed.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify Morein, Johns, Dye so pitch value has distance in address units between 2 of plurality of subpixels because Liang suggests this value is needed in order to shrink pitch to minimum, hence obtaining very good sharpness of frame and increasing area and window ratio of display pixels. Resolution of display can thus be enhanced [0015].

25. As per Claims 6, 12, 18, and 25, Morein does not teach CPU calculating physical address within frame buffer using pitch value of frame buffer as pitch of virtual frame buffer. However, Dye teaches CPU 128 calculating physical address within frame buffer

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110 using pitch value of frame buffer as pitch of virtual frame buffer 116 (c. 3, ll. 49-51; c. 12, ll. 1-24). This would be obvious for the same reasons given for Claim 5.

However, Morein and Dye do not teach pitch value comprises distance between two of the plurality of subpixels. But, Liang teaches this [0002], as discussed for Claim 5.

26. Claims 7, 8, 14, 20, 27, and 38-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morein (US006188394B1) and Johns (US006366289B1) in view of Baldwin (US005594854A), further in view of Fuchs.

27. As per Claims 7 and 38, Morein and Johns are relied on for teachings above for Claim 1. The combination of Morein and Johns teaches plurality of subpixels corresponding to pixel are within virtual frame buffer, as discussed for Claim 1.

But, Morein and Johns don't teach plurality of subpixels corresponding to pixel of virtual frame buffer have physical addresses that are nearby each other. But, Baldwin teaches buffer must reside at contiguous physical addresses, if virtual memory buffer maps to non-contiguous physical memory, then buffer must be divided into sets of contiguous physical memory pages (c. 18, ll. 45-52). So, data of virtual frame buffer have physical addresses that are nearby each other (c. 18, ll. 35-52). Baldwin teaches performing subpixel correction (c. 34, ll. 61-67).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify Morein and Johns so data of virtual frame buffer have physical addresses that are nearby each other because Baldwin suggests this is needed because data in physical memory needs to be transferred together (c. 18, ll. 35-52).

But, Morein, Johns, and Baldwin do not teach each physical address corresponds to one of plurality of subpixels. But, Fuchs teaches pixel address (x, y) is subdivided into

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grid of subpixels so each subpixel has address of form (x+xoffset, y+yoffset) (p. 119, second col., 4<sup>th</sup> para). So, each subpixel in grid of multiple subpixels has different xoffset and different yoffset, and so each subpixel has different physical address.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify Morein, Johns, and Baldwin so each physical address corresponds to one of the plurality of subpixels because Fuchs teaches advantage of knowing location of sample points within pixel at which to sample in order to perform anti-aliasing (p. 119, 2<sup>nd</sup> col., 3<sup>rd</sup> - 4<sup>th</sup> para.).

28. As per Claims 8, 14, 20, 27, Morein does not teach physical addresses are based on base physical address which corresponds to memory address. But, Johns teaches this (c. 10, ll. 26-35).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Morein so physical addresses are based on base physical address because Johns teaches base physical address is needed as reference starting point, all addresses can be determined by their offsets from base physical address (c. 10, ll. 26-35).

29. As per Claim 39, it is similar in scope to Claim 32 except it is for writing pixel value and subpixels have nearby physical addresses. Morein teaches writing pixel value (c. 2, ll. 15-19).

But, Morein does not teach subpixels have nearby physical addresses. But, incorporating teachings from Baldwin and Fuchs teaches this, as discussed for Claim 7.

30. As per Claims 40-42, these claims are similar in scope to Claims 33-35 respectively, and therefore are rejected under the same rationale.

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31. Claims 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morein (US006188394B1), Fuchs, and Johns (US006366289B1).

32. As per Claim 28, Morein teaches reading frame buffer (sample memory 38, Fig. 2; c. 2, ll. 19-23; c. 4, ll. 9-13), comprising receiving address corresponding to pixel (c. 2, ll. 18-20); transforming received address into at least 1 subpixel (sample) address (c. 2, ll. 20-23; c. 2, ll. 25-31); reading at least 2 subpixels from frame buffer using at least 1 subpixel address (c. 4, ll. 9-13), frame buffer is single memory comprising plurality of pixels, each pixel has plurality of subpixels (c. 5, ll. 44-47; c. 2, ll. 25-31); and blending at least two subpixels to create pixel value for pixel (c. 2, ll. 25-31). Frame buffer stores uncompressed set of subpixels (c. 5, ll. 57-63).

But, Morein does not teach mapping pixel address into plurality of subpixel addresses; transforming received address into multiple subpixel addresses, wherein each of multiple subpixel addresses comprises mapped subpixel address; using at least 2 of multiple subpixel addresses to read at least 2 subpixels. But, Fuchs teaches pixel address (x, y) is subdivided into grid of subpixels so each subpixel has address of form (x+xoffset, y+yoffset) (p. 119, 2<sup>nd</sup> col., 4<sup>th</sup> para). So, each subpixel in grid of multiple subpixels has different xoffset and different yoffset, so each subpixel has different address. So, received address (x, y) is mapped into multiple subpixel addresses and each of multiple subpixel addresses comprises mapped subpixel address since each of multiple subpixels has different address in form (x+xoffset, y+yoffset) since each of multiple subpixels has different xoffset and different yoffset. Fuchs teaches using 2 subpixel addresses to read 2 subpixels (p. 119, 2<sup>nd</sup> col., 4<sup>th</sup> para).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Morein to include mapping pixel address into plurality of subpixel addresses; transforming received address into multiple subpixel addresses, wherein each of multiple subpixel addresses comprises mapped subpixel address; using at least 2 of multiple subpixel addresses to read at least 2 subpixels because Fuchs suggests advantage of knowing location of sample points within pixel at which to sample in order to perform anti-aliasing (p. 119, 2nd col., 3rd and 4th para.).

However, Morein and Fuchs do not teach that the address is associated with a virtual frame buffer. However, Johns teaches this limitation, as discussed for Claim 1.

33. As per Claim 29, Morein teaches supplying the pixel value as if it were a pixel value at the received address (c. 4, ll. 6-14).

34. As per Claim 30, Morein teaches writing frame buffer (38, Fig. 2) having receiving address and pixel value from computer program (84, Fig. 4; c. 2, ll. 19-21; c. 8, ll. 15-27), computer program supplying address and pixel value as if accessing frame buffer that does not comprise subpixels (samples); transforming received address into at least one subpixel address; writing pixel value to frame buffer as multiple subpixel values using subpixel address (c. 2, ll. 19-23, 25-31), frame buffer is single memory having plurality of pixels (c. 5, ll. 44-47), each pixel has plurality of subpixels (c. 5, ll. 39-44).

But, Morein does not teach mapping pixel address into plurality of subpixel addresses; transforming received address into multiple subpixel addresses, wherein each of multiple subpixel addresses comprises mapped subpixel address; writing pixel value as multiple subpixel values using multiple subpixel addresses. But, Fuchs teaches this (p. 119, 2nd col., 4th para.). This would be obvious for reasons for Claim 28.



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However, Morein and Fuchs do not teach that the address is associated with a virtual frame buffer. However, Johns teaches this, as discussed in rejection for Claim 1.

35. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morein (US006188394B1), Fuchs and Johns (US006366289B1) in view of Toji (US007158148B2).

Morein, Fuchs, and Johns are relied on for teachings relative to Claim 30.

But, Morein, Fuchs, Johns do not teach modifying one of multiple subpixel values in frame buffer based upon pixel value of surrounding pixel. But, Toji teaches this (c. 40, ll. 40-47).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Morein, Fuchs, and Johns to include modifying at least one of multiple subpixel values in frame buffer based upon pixel value of surrounding pixel because Toji suggests allowing smoother image to be displayed (c. 2, ll. 58-65).

#### ***Allowable Subject Matter***

36. Claims 24, 36, 37, 43, and 44 are objected to as being dependent upon a rejected claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

#### ***Conclusion***

Applicant's amendment necessitated new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

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TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JONI HSU whose telephone number is (571)272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on 571-272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JH

/Kee M Tung/

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Supervisory Patent Examiner, Art Unit 2628